REMARKS

Claims 1, 10-16, 18, and 26-27 are amended. No new subject matter is added. Claims 1-20 and 26-27 remain in the case for consideration. Reconsideration and allowance of the claims is respectfully requested in light of the following remarks.

Objection to the Drawings

The drawings are objected to for failing to show every feature specified in the claims. In particular, claims 1, 10, and 15 recite a plurality of sector units or sectors, and the drawings do not show a plurality of sector units or sectors. Consequently, the feature of "a plurality of sector units" or "a plurality of sectors" is cancelled from claims 1, 10, and 15. Claims 11-14 and 26 are amended for consistency with claim 10. Claim 16 is amended for consistency with claim 15. No new subject matter is added.

Furthermore, it is alleged that the drawings fails to show the features recited in claims 18 and 27. In particular, the feature of a cell array block arranged in an (M x N) array with M and N both at least equal to two and the feature of a column decoder block arranged in a (P x N) array with P at least equal to one is allegedly not shown by the drawings. The applicants disagree.

FIG. 3 of the application as originally filed shows a sector 100 having a cell array block 101 and a column decoder block 103. The applicants show in FIG. 3 that the memory cells are arranged at the intersection of the word lines WL and the bitlines BL. The first word line is labeled WL0 and the last word line is labeled WLn-1. The first bit line is labeled BL0 and the last word line is labeled BLm-1. Thus, the memory cells shown in FIG. 3 are labeled from M1 (upper left hand corner) to Mnm (lower right hand corner).

It is also shown in FIG. 3 that the transistors in the column decoder block 103 are arranged such that there is a transistor that corresponds to each of the bit lines BL0 to BLm-1. Thus, FIG. 3 shows that the "m-1" dimension of the column decoder block 103 is the same size as the "m-1" dimension of the cell array block 101.

The "n", "m", "n-1", and "m-1" notation is extremely well-known in the art, and those of ordinary skill know that using such notation does not limit the size of the array, since m and n may be chosen to be arbitrarily large. Thus, although FIG. 3 is illustrated relatively "small" so that it may be conveniently shown on a page of paper, the notation used illustrates

that the maximum size of the cell array block and the column decoder block is not limited by FIG. 3.

Furthermore, those of ordinary skill in the art also know that the "n", "m", "n-1", and "m-1" notation used in FIG. 3 limits the minimum size of the cell array block and the column decoder block only to values that give sensible results. For example, FIG. 3 labels the first word line as WL0 and the first bit line as BL0. Those of ordinary skill know that this notation does not mean that there are zero word lines and zero bit lines, but that "0" is often chosen as a label for the first bit line or first word line in a series, i.e., the "zeroth" bit line.

Finally, FIG. 3 makes frequent use of the (* * *) notation throughout. Those of ordinary skill know these symbols, especially when used in conjunction with variable "m" and "n" notation, indicate repetitive structures or quantities that may be, but do not necessarily have to be, present.

Returning to the language of the disputed features, the applicants have amended claims 18 and 27 to read that the plurality of memory cell transistors of the cell array block are arranged in a (M x N) array and the plurality of column decoder transistors of the column decoder block are arranged within a (N x N) array adjacent to the cell array block, where M and N are at least equal to two. These features are fully supported by the application as originally filed, eg., at FIG. 3. Those of ordinary skill know that the (M x N) notation is frequently used to specify the number of rows and columns in an array. The applicant may be his or her own lexicographer as long as the meaning assigned to the term is not repugnant to the term's well-known usage. MPEP 2111.02, *citing* In re Hill, 161 F.2d 367 (CCPA 1947).

FIG. 3 illustrates that the memory cell array block 101 may be small enough to contain only the transistors M1, M2, M11, and M21. These transistors are shown at the intersection of the word lines WL0 and WL1 with the bit lines BL0 and BL1. Thus, FIG. 3 illustrates the recited feature of the plurality of memory cell transistors of the cell array block arranged in a (M x N) array, where M and N are at least equal to two.

FIG. 3 illustrates that the column decoder block 103 may be small enough to contain only the transistors T1 and T2. These transistors are shown at the intersection of the bit lines BL0 and BL1 with the signals YPASS0 and YPASS1. Thus, FIG. 2 shows the recited feature of the plurality of column decoder transistors of the column decoder block arranged within a (N x N) array adjacent to the cell array block, where N is at least equal to two.

The drawings are also objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "100" and "101" have both been used to designate the memory cell array block. Although the Examiner does not specifically state which drawing he is referring to, it is believed that the objection is to FIG. 3. Thus, a replacement sheet for FIG. 3 is submitted in the Appendix following page 12 of this paper. The replacement sheet clearly shows that the reference character "100" now only refers to the sector structure and not to the column decoder block "101".

For the above reasons, the applicants submit that the objection to the drawings is overcome.

Rejections under 35 USC § 112, first paragraph

Claims 1-17 and 26-27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. It is alleged that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The applicants disagree.

Although the Examiner has indicated that features of the claims fail to meet the enablement requirement, the Examiner has stated, for each rejection, that the disputed feature recited in the claims is either "not shown in the drawings" or "not described in the specification". Thus, the Examiner is actually characterizing the features of the claims as failing the written description requirement, which is also a requirement of 35 USC 112, first paragraph. However, the written description requirement is separate and distinct from the enablement requirement. MPEP 2161, *citing* In re Barker, 559 F.2d 588 (CCPA 1977). Thus, the applicants will address both the written description requirement and the enablement requirement in the paragraphs below.

Claims 1-17 and 26-27 are rejected because the recited plurality of sectors "is not shown in the drawings". As explained above, claims 1, 10, and 15 were amended to remove the feature of a plurality of sectors. The other claims were amended for consistency with claims 1, 10, and 15. No new subject matter was added. Since the feature of a plurality of sectors no longer appears in the claims, the rejections that are based upon this feature is overcome.

Claim 1-17 and 26-27 are also rejected because it is alleged that the feature of "electrically [erasing] all the memory cell transistors in sectors together" is not described in the specification. To the contrary, this feature is described in the specification as originally filed at, e.g, page 8, lines 12-15. Thus, the written description requirement is met.

Claims 18-20 are rejected because the feature of the (M x N) array with M and N both at least equal to two is not shown in the drawings and not described in the specification. To the contrary, it was explained above how the feature of a (M x N) memory cell array is adequately described in FIG. 3. Furthermore, it is well accepted that a satisfactory description may be in the claim or ***any other portion of the originally filed application*** (MPEP 2163, Section I, emphasis added). Information contained in any one of the specification, claims, ***or drawings*** of the application as filed may be added to any other part of the application without introducing new matter (MPEP 2163.06, emphasis added). Thus, the written description requirement is met.

Finally, with regard to the enablement requirement under 35 USC § 112, first paragraph, detailed procedures for making and using the invention may not be necessary if the description of the invention itself is sufficient to permit those skilled in the art to make and use the invention (MPEP 2164).

The feature of "electrically [erasing] all the memory cell transistors in sectors together" is described by the applicants as being possible because all the memory cell transistors share the same bulk region, and the applicants describe this in detail (see, e.g., page 8, lines 12-24). The applicants submit that this description of the invention is sufficient to permit those skilled in the art to make and use the invention. Thus, the recited feature fulfills the enablement requirement.

As amended, the feature of "the plurality of memory cell transistors of the cell array block are arranged in a (M x N) array and the plurality of column decoder transistors of the column decoder block are arranged within a (N x N) array adjacent to the cell array block, where M and N are at least equal to two" is alleged to fail the enablement requirement. It was explained above how this feature is adequately described by FIG. 3 of the original application. Furthermore, this feature is directed toward the arrangement of transistors on a semiconductor substrate. The applicants submit that the description provided in FIG. 3 of the application as originally filed would permit those skilled in the art to make and use the invention. Thus, the recited feature fulfills the enablement requirement.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-20 and 26-27 of the application as amended is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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Annotated Sheet Showing Changes

FIG.3